Programming the AMD Instinct™ MI300 APU
Or everything you wanted to know about APU programming but were afraid to ask
Presented at ESPM2 at SC23
LLNL's El Capitan Exascale will be powered by the AMD Instinct™ MI300 APU: “MI300A”

- MI300A is an APU, with AMD CDNA™ 3 GPUs, Zen 4 CPUs, cache memory, and HBM chiplets in a single package
- 24 Zen4 CPU cores
- 128 GiB of HBM3

“It’s much easier to program”
AGENDA

MI300A Hardware: What is an APU?

How can programmers prepare for the APU architecture?

Simple examples in HIP, RAJA, Kokkos, OpenMP

What are the performance opportunities of an APU?

Removing redundant memory copies
Fine-grained interleaving between CPU and GPU
Scheduling concurrent work
Efficient memory allocations and kernel launches
AMD CDNA™ 2 Coherent Memory Architecture ▶ AMD CDNA™ 3 Unified Memory APU Architecture

- Eliminate Redundant Memory Copies
- No programming distinction between host and device memory spaces
- High performance, fine-grained sharing between CPU and GPU processing elements
- Single process can address all memory, compute elements on a socket
## APU Programming Model

<table>
<thead>
<tr>
<th>CPU CODE</th>
<th>GPU CODE</th>
<th>APU CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>double* in_h = (double*)malloc(Msize); double* out_h = (double*)malloc(Msize);</td>
<td>double* in_h = (double*)malloc(Msize); double* out_h = (double*)malloc(Msize); hipMalloc(&amp;in_d, Msize); hipMalloc(&amp;out_d, Msize);</td>
<td>double* in_h = (double*)malloc(Msize); double* out_h = (double*)malloc(Msize);</td>
</tr>
<tr>
<td>for (int i=0; i&lt;M; i++) // initialize in_h[i] = ...;</td>
<td>for (int i=0; i&lt;M; i++) // initialize in_h[i] = ...; hipMemcpy(in_d, in_h, Msize);</td>
<td>for (int i=0; i&lt;M; i++) // initialize in_h[i] = ...;</td>
</tr>
<tr>
<td>cpu_func(in_h, out_h, M);</td>
<td>gpu_func&lt;&lt;&lt;&gt;&gt;(in_d, out_d, M); hipDeviceSynchronize(); hipMemcpy(out_h, out_d, Msize);</td>
<td>gpu_func&lt;&lt;&lt;&gt;&gt;(in_h, out_h, M); hipDeviceSynchronize();</td>
</tr>
<tr>
<td>for (int i=0; i&lt;M; i++) // CPU-process ... = out_h[i];</td>
<td>for (int i=0; i&lt;M; i++) // CPU-process ... = out_h[i];</td>
<td>for (int i=0; i&lt;M; i++) // CPU-process ... = out_h[i];</td>
</tr>
</tbody>
</table>

- GPU memory allocation on Device
- Explicit memory management between CPU & GPU
- Synchronization Barrier
GPU CODE

double* in_h = (double*)malloc(Msize);
double* out_h = (double*)malloc(Msize);
hipMalloc(&in_d, Msize);
hipMalloc(&out_d, Msize);

for (int i=0; i<M; i++) //initialize
  in_h[i] = ...;
hipMemcpy(in_d, in_h, Msize);
gpu_func<<<>(in_d, out_d, M);
hipDeviceSynchronize();
hipMemcpy(out_h, out_d, Msize);

for (int i=0; i<M; i++) // CPU-process
  ... = out_h[i];

• GPU memory allocation on Device
• Explicit memory management between CPU & GPU
• Synchronization Barrier

<table>
<thead>
<tr>
<th>Operation</th>
<th>MI250X (MCM)</th>
<th>MI300A</th>
</tr>
</thead>
<tbody>
<tr>
<td>H2D Copy</td>
<td>O(10) GB/s</td>
<td>O(TB/s)</td>
</tr>
</tbody>
</table>
APU PROGRAMMING: PERFORMANCE IMPLICATIONS

APU CODE

double* in_h = (double*)malloc(Msize);
double* out_h = (double*)malloc(Msize);

for (int i=0; i<M; i++) //initialize
    in_h[i] = ...;

gpu_func<< (in_h, out_h, M);

hipDeviceSynchronize();

for (int i=0; i<M; i++) // CPU-process
    ... = out_h[i];

---

• GPU memory allocation on Device
• Explicit memory management between CPU & GPU
• Synchronization Barrier

<table>
<thead>
<tr>
<th>Operation</th>
<th>MI250X (MCM)</th>
<th>MI300A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coherent Access</td>
<td>O(10) GB/s</td>
<td>N/A</td>
</tr>
</tbody>
</table>
## PROGRAMMING ACROSS FRAMEWORKS/COMPILERS

<table>
<thead>
<tr>
<th>OpenMP® CODE</th>
<th>RAJA CODE</th>
<th>KOKKOS CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>#pragma omp requires unified_shared_memory</td>
<td>double* in_h = (double*)malloc(Msize);</td>
<td>double* in_h = (double*)malloc(Msize);</td>
</tr>
<tr>
<td>double* out_h = (double*)malloc(Msize);</td>
<td>double* out_h = (double*)malloc(Msize);</td>
<td>double* out_h = (double*)malloc(Msize);</td>
</tr>
<tr>
<td>for (int i=0; i&lt;M; i++) // initialize</td>
<td>in_h[i] = ...;</td>
<td>in_h[i] = ...;</td>
</tr>
<tr>
<td>in_h[i] = ...;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>#pragma omp target</td>
<td>RAJA::forall&lt; exec_policy &gt;(arange, [=] (int i) { ... });</td>
<td>Kokkos::parallel_for(M, [=] (const int i){ ... });</td>
</tr>
<tr>
<td>{ ... }</td>
<td></td>
<td>Kokkos::fence();</td>
</tr>
<tr>
<td>for (int i=0; i&lt;M; i++) // CPU-process</td>
<td>for (int i=0; i&lt;M; i++) // CPU-process</td>
<td>for (int i=0; i&lt;M; i++) // CPU-process</td>
</tr>
<tr>
<td>... = out_h[i];</td>
<td>... = out_h[i];</td>
<td>... = out_h[i];</td>
</tr>
</tbody>
</table>

- **GPU memory allocation on Device**
- **Explicit memory management between CPU & GPU**
- **Synchronization Barrier**
• Runtime knows it can omit copies and map clauses
• (Implicit) Synchronization Barrier

```c
#pragma omp requires unified_shared_memory

double* in_h = (double*)malloc(Msize);
double* out_h = (double*)malloc(Msize);

for (int i=0; i<M; i++) //initialize
    in_h[i] = ...;

#pragma omp target
{
    ...
}

for (int i=0; i<M; i++) // CPU-process
    ... = out_h[i];
```
Synchronization barrier requiring GPU kernel to complete

```
GPU CODE W/ MI300A

double* in_h = (double*)malloc(Msize);
double* out_h = (double*)malloc(Msize);

for (int i=0; i<M; i++) //initialize
    in_h[i] = ...;

gpu_func<<(in_h, out_h, M);
hipDeviceSynchronize();

for (int i=0; i<M; i++) // CPU-process
    ... = out_h[i];
```

- Synchronization barrier requiring GPU kernel to complete
**RESEARCH: OVERLAP CPU & GPU AT CACHE LINE GRANULARITY**

**APU CODE W/ MI300A**

```c
double* in_h = (double*)malloc(Msize);
double* out_h = (double*)malloc(Msize);
int* flag = (int*)malloc(Isize);

for (int i=0; i<M; i++) //initialize
    in_h[i] = ...;   flag[i] = 0;
gpu_func<<(in_h, out_h, M);
hipDeviceSynchronize();

for(int j = 0; j<Isize; j++){
    while(atomic_load(&flag[j]) == 0){}
    post_process(out_h[j]); // CPU-process
}
```

- Spin-loop on flag
- No Synchronization barrier; GPU kernel not required to complete
- Requires fine-grained memory allocations (128B)
ACCELERATING LIBRARY PERFORMANCE

INTELLIGENT OFFLOAD

```c
double* in_h = (double*)malloc(Msize);
double* out_h = (double*)malloc(Msize);

for (int i=0; i<M; i++) //initialize
    in_h[i] = ...;

Library_Function (in_h, out_h, M);
```
• AMD providing support for advanced C++ in LLVM: today, entirely Open Source Software (OSS)
  • Only supports par_unseq acceleration currently
  • https://discourse.llvm.org/t/rfc-adding-c-parallel-algorithm-offload-support-to-clang-llvm/72159/3
  • Re-uses HIP support in CLANG/LLVM and algorithms from libraries (rocThrust)
  • Available today: https://github.com/ROCmSoftwarePlatform/roc-stdlib
    • More than 23 applications tested and running (LULESH, etc.)

```cpp
1 std::transform( // needs <algorithm>
2     std::execution::par_unseq, // <-- needs <execution>
3     indices.begin(), indices.end(), grid.begin(),
4     [](size_t index){
5         return expensive_calculation(index);
6     }
7 );
```
CONCLUSIONS AND RECOMMENDATIONS

• MI300A is an APU with a unified memory space between CPUs and GPUs
• Portable programming paradigms such as RAJA, Kokkos, and OpenMP® should not require code refactoring
• HIP code should compile and run ‘out-of-the-box’
• HIP code can be optimized to:
  1) Remove redundant memory allocations and migrations
  2) Perform fine-grained (cache line) sharing between CPU and GPU
• Stay tuned for advanced capabilities such as:
  • Automatic library offload
  • Standard parallelism
Thank You and Attribution

This content was developed by many at AMD:

- Nick Malaya
- Sam Antao
- Ian Bogle
- Paul Bauman
- Bill Brantley
- Noel Chalmers
- Nick Curtis
- Austin Ellis
- Alessandro Fanfarillo
- Joe Greathouse
- Leopold Grinberg
- Michael Klemm
- Felix Kuehling
- Jakub Kurzak
- George Markomanolis
- Damon McDougall
- Jose Noudohouenou
- Corbin Robeck
- Michael Rowan
- Gina Sitaraman
- Noah Wolfe
- Johannes Dieterich
- Alex Voicu
DISCLAIMER

©2023 Advanced Micro Devices, Inc. All rights reserved.

AMD, the AMD Arrow logo, EPYC™, Instinct™ and combinations thereof are trademarks of Advanced Micro Devices, Inc. The OpenMP name and the OpenMP logo are registered trademarks of the OpenMP Architecture Review Board. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

The information presented in this document is for informational purposes only and may contain technical inaccuracies, omissions, and typographical errors. The information contained herein is subject to change and may be rendered inaccurate for many reasons, including but not limited to product and roadmap changes, component and motherboard version changes, new model and/or product releases, product differences between differing manufacturers, software changes, BIOS flashes, firmware upgrades, or the like. Any computer system has risks of security vulnerabilities that cannot be completely prevented or mitigated. AMD assumes no obligation to update or otherwise correct or revise this information. However, AMD reserves the right to revise this information and to make changes from time to time to the content hereof without obligation of AMD to notify any person of such revisions or changes.

THIS INFORMATION IS PROVIDED ‘AS IS.’ AMD MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE CONTENTS HEREOF AND ASSUMES NO RESPONSIBILITY FOR ANY INACCURACIES, ERRORS, OR OMISSIONS THAT MAY APPEAR IN THIS INFORMATION. AMD SPECIFICALLY DISCLAIMS ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, OR FITNESS FOR ANY PARTICULAR PURPOSE. IN NO EVENT WILL AMD BE LIABLE TO ANY PERSON FOR ANY RELIANCE, DIRECT, INDIRECT, SPECIAL, OR OTHER CONSEQUENTIAL DAMAGES ARISING FROM THE USE OF ANY INFORMATION CONTAINED HEREIN, EVEN IF AMD IS EXPRESSLY ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.
Pillars of Exascale Software

OpenMP

Established Leader in Compiler Directives

HIP

Open & Portable GPU Programming

TensorFlow, PyTorch

ML Frameworks

Unlocked

100% Open Software on Community Standards

Unified CPU + GPU Tools